Assignee: Intel Corporation
Docket No.: 2207/7942

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS	:	Deborah T. Marr, et al.
SERIAL NO.	:	09/490,172
FILED	:	January 22, 2000
FOR	:	ESTABLISHING THREAD PRIORITY IN A PROCESSOR OR THE LIKE
GROUP ART UNIT	:	2171
EXAMINER	:	Susan (Te Y.) Chen

M/S: APPEAL BRIEF - PATENT
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

RESPONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF

Dear Sir:

The following is submitted in response to the Notice of Non-Compliant Appeal Brief dated July 6, 2007.

It is noted that Applicants have already filed a Reply Brief on July 19, 2007.

Changes to Section 5 of the Appeal Brief appear on page 2.

Amendments to the presentation of the claims with their status is presented in the Appendix. It is noted that Section 3 of the Appeal Brief as filed identified the status of the claims.

Please change Section 5 to read as follows:

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

Embodiments of the present invention pertain to establishing priority of a thread in a multi-threaded processor. A counter may be provided to store a value that assists in designating an amount of time that one thread will have priority over others. The value stored in the counter may be selected for each thread so as to give some threads a greater amount of priority (e.g., in access to a resource) compared to others.

In the embodiment of claim 1, a method is provided including assigning a value in memory to indicate which of a plurality of threads executed by a single processor has a higher priority (see, e.g., pg. 6, lines 4-6 and elements 3 and 4 in Fig. 1). In a next operation, a resource is allocated between the plurality of threads depending on a priority assigned to each thread (see, e.g., pg. 8, lines 14-21; an example of a resource is shown in Fig. 4 (element 81) and pg. 9, lines 6-19). In the allocation, a counter is provided with a predetermined value for the plurality of threads (see, e.g., Fig. 3, element 68), the value being selected by control logic depending on the priority assigned to each thread (see, e.g., pg. 7, line 21 to pg. 8, line 15).

In the embodiment of claim 10 a method is provided including assigning a value in an APIC TPR (Advanced Programmable Interrupt Controller – Task Priority Register) register for a thread via execution of operating system code to indicate which of a plurality of threads executed by said single processor has a higher priority (see, e.g., elements 3 and 4 and pg. 6, lines 4-22). In a next operation a resource is allocated between the plurality of threads depending on a priority assigned to each thread (see, e.g., pg. 8, lines 14-21; an example of a resource is shown in Fig. 4 (element 81) and pg. 9, lines 6-19). In the allocation, a counter is provided with a

predetermined value for said plurality of threads (see, e.g., Fig. 3, element 68), the value being selected by control logic depending on the priority assigned to each thread, said counter being used in said allocating operation (see, e.g., pg. 7, line 21 to pg. 8, line 15).

In the embodiment of claim 11, an apparatus is provided comprising a memory to store a value to indicate which of a plurality of threads to be executed by a single processor has a higher priority (see, e.g., pg. 6, lines 4-6 and elements 3 and 4 in Fig. 1). A resource is allocated between the plurality of threads depending on a priority assigned to each thread in said memory (see, e.g., pg. 8, lines 14-21; an example of a resource is shown in Fig. 4 (element 81) and pg. 9, lines 6-19). A counter loaded with a predetermined value by control logic for each thread in the memory depending on the priority assigned (see, e.g., Fig. 3, element 68). The counter is used to allocate said resource between said plurality of threads (see, e.g., pg. 7, line 21 to pg. 8, line 15).

In the embodiment of claim 20, an apparatus is provided for establishing thread priority in a single processor. The apparatus includes an APIC TPR register for a thread wherein execution of operating system code causes a value to be stored in said register to indicate which of a plurality of threads to be executed by the single processor has a higher priority (see, e.g., elements 3 and 4 and pg. 6, lines 4-22). A resource allocated between said plurality of threads depending on a priority assigned to each thread in said memory (see, e.g., pg. 8, lines 14-21; an example of a resource is shown in Fig. 4 (element 81) and pg. 9, lines 6-19). A counter loaded with a predetermined value by control logic for each thread in said memory (see, e.g., Fig. 3, element 68), said value being selected depending on the priority assigned, said counter being used to allocate said resource between said plurality of threads (see, e.g., pg. 7, line 21 to pg. 8, line 15).

CONCLUSION

Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's decision rejecting claims 1, 3-11, and 13-21 under 35 U.S.C. § 103(a) direct the Examiner to pass the case to issue.

The Commissioner is hereby authorized to charge any fees which may be necessary for consideration of this paper to Kenyon & Kenyon Deposit Account No. 11-0600. A copy of this sheet is enclosed for that purpose.

Respectfully submitted,

Date: August 6, 2007

Shawn W. O'Dowd
(Reg. # 34,687)

KENYON & KENYON LLP
1500 K Street, NW
Suite 700
Washington, DC 20005
(202) 220-4200 telephone
(202) 220-42501 facsimile
DC1-670906